PHASE-CHANGE MEMORY

Phase-change heterostructure enables ultralow noise and drift for memory operation

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Artificial intelligence and other data-intensive applications have escalated the demand for data storage and processing. New computing devices, such as phase-change random access memory (PCRAM)–based neuro-inspired devices, are promising options for breaking the von Neumann barrier by unifying storage with computing in memory cells. However, current PCRAM devices have considerable noise and drift in electrical resistance that erodes the precision and consistency of these devices. We designed a phase-change heterostructure (PCH) that consists of alternately stacked phase-change and confinement nanolayers to suppress the noise and drift, allowing reliable iterative RESET and cumulative SET operations for high-performance neuro-inspired computing. Our PCH architecture is amenable to industrial production as an intrinsic materials solution, without complex manufacturing procedure or much increased fabrication cost.

The rapid development of artificial intelligence (AI), big data analytics, and supercomputing demands a fundamental change in the current computing systems based on von Neumann architecture (*1*–*7*), which is characterized by physically separated processing and storage units. Their intercommunication across bandwidth-limited and energy-inefficient interconnects constitutes a bottleneck for data shuffling, leading to a 40% power waste. Chalcogenide phase-change materials (PCMs)–based random-access memory (PCRAM) (*7*–*14*), available as storage-class memory in the memory market (*15*), can mitigate to some extent the performance mismatch between dynamic random access memory (DRAM) and flash-memory–based solid-state drives. But to fundamentally break the aforementioned bottleneck, non–von Neumann computing architecture that unifies computing with storage in memory cells, such as neuro-inspired computing (*1*–*7*), needs to be pursued. Resistive memories such as PCRAM are a promising route for the implementation of this new form of computing (*2*–*7*). This, however, sets a high bar for the performance of PCRAM.

PCRAM products currently use $Ge_2Sb_2Te_5$ (GST) as the core material for memory programming. Digital information is encoded through reversible transformation between the amorphous and crystalline phases of GST. The unconstrained three-dimensional phase transitions, crystallization (SET operation), and melt-quenched amorphization (RESET operation) cause composition deviations and structural variations upon extensive cycling. This results in large fluctuations in electrical resistance of both the SET (crystalline) and RESET (amorphous) states (*16*). Structural relaxation also takes place in amorphous GST, resulting in the steady increase in electrical resistance with time at ambient temperatures that is known as the resistance drift (*17*). For binary storage, these noise and drift issues are not critical because the resistance contrast between amorphous and crystalline GST is greater than two orders of magnitude and clearly distinguishable at all times. However, the strong intra- and intercell variability becomes a formidable challenge when it comes to the implementation of neuro-inspired computing as in-memory computing (*18*–*21*), deep neural networks (*22*), and spiking neural networks (*23*–*25*).

Recent device advances to address this challenge—which include the mixed-precision in-memory computing scheme (*18*), the projected phase-change memory scheme (*26*, *27*), and the multi-PCRAM cells scheme (*22*, *23*)—have resulted in much improvement in the speed-up and energy-saving factors for key computing tasks, such as vector-matrix multiplications (*18*), pattern recognitions (*22*), temporal correlation detection (*28*), and other machine-learning tasks (*29*). However, these remedies (i) mostly improve the RESET aspect and cannot resolve the randomness issue associated with the SET operations for machine-learning tasks that require high accuracy and consistency, (ii) complicate the chip-system architecture and the inherent working mode, hindering its integration into mass-produced chips, and (iii) are largely extrinsic help from the device setup and connection standpoint. Therefore, an intrinsic solution that improves each and every PCRAM cell is a pressing need (*30*). One solution is an innovative materials design that enables low noise, small drift, long cycling endurance, fast switching, and high energy efficiency. We propose and have demonstrated a phase-change heterostructure (PCH) that simultaneously resolves all of these critical issues, opening a different avenue toward high-performance phase-change computing chips.

Design principles and fabrication of a PCH device

For typical T-shaped phase-change devices fabricated by use of the 0.13-μm node complementary metal-oxide semiconductor (CMOS) technology, the programming (amorphous-crystalline phase transformation) region in the PCM layer forms a mushroom-like shape (Fig. 1A). To avoid the long-distance atomic transport along the pulsing direction, the conventional monolithic PCM needs to be subdivided into compartments. We therefore replaced the active layer with a multilayer PCH composed of alternately deposited nanolayers of a confinement material (CM) and a PCM (Fig. 1B). The materials selection was based on the following design principles, leading to six criteria that should be met simultaneously for superior device performances. The performance includes not only low variability and drift but also long cycling endurance, low power consumption, and high switching speed.

First, we required the CM layers to be dynamically robust in dense grids, acting as effective diffusion barriers against long-range atomic transport along the pulsing direction upon extensive cycling. The CM crystal should therefore have a much higher melting temperature (T_m) and smaller in-plane lattice parameter than that of the PCM layer. Second, the CM should be chemically unreactive and weakly coupled (for example, through weak covalent and/or van der Waals interactions) with the PCM layer, to keep the heterostructure interfaces intact at all operation temperatures. Strong CM-PCM interfacial bonding needs to be avoided because it may pin down the outer atomic layers in the PCM slab toward its crystalline structure, making the remaining amorphous fraction difficult to be sustained at nanoscale (*31*, *32*). Third, the CM layers should have local (short to medium range) atomic arrangements (such as octahedral motifs) similar

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to that of the crystalline PCM counterpart, which could help speed up crystallization of the amorphous PCM. Fourth, the CM layers need to be thermally resistive to serve as effective barriers to prevent through-plane heat loss during programming, thus reducing the required programming bias (energy). Fifth, the CM layers should have similar electrical resistivity as compared with that of the PCM layers, maintaining the resistance window suitable for programming. Sixth, the CM selection should be compatible with the current PCMs and CMOS technology, without involving undesirable or excessive elements.

After we screened potential candidate systems on the basis of the above criteria, we found that the transition-metal dichalcogenides MX_2—with X = Te and M = Ti, Zr, Ni, or Mo, for example—were suitable choices for the CM. Although there are plenty of MX_2-PCM combinations, we used CM = $TiTe_2$ and PCM = Sb_2Te_3 because this combination was experimentally verified to be weakly coupled (*33*). The $TiTe_2$/Sb_2Te_3 couple satisfies all our criteria because $TiTe_2$ has a much higher T_m of ~1470 K, a lower thermal conductivity of ~0.12 W m^{-1} K^{-1}, a comparable electrical resistivity of ~1.3×10^{-6} ohm m, and a similar octahedral arrangement with a smaller in-plane lattice parameter of ~3.77 Å (Fig. 1C) in comparison with Sb_2Te_3 (~900 K, ~0.78 W m^{-1} K^{-1}, ~3×10^{-5} ohm m, and ~4.26 Å, respectively) (Fig. 1D) (*33*). Density functional theory (DFT) calculations (*34*) indicate a more favorable cohesive energy of $TiTe_2$ (–0.694 eV per atom) as compared with Sb_2Te_3 (–0.119 eV per atom). Crystal orbital Hamilton population (COHP) analyses (*34*) indicate that both $TiTe_2$ (Fig. 1C) and Sb_2Te_3 (Fig. 1D) are chemically robust, as evidenced by the absence of antibonding interaction at the Fermi level. In particular, the Ti–Te bonds are of high chemical strength owing to the pure stabilizing contribution below the Fermi level.

We fabricated the T-shaped $TiTe_2$/Sb_2Te_3 PCH device using the 0.13-μm node CMOS technology with a tungsten bottom electrode contact (BEC) ~190 nm in diameter (Φ) (*34*). We deposited the PCH film, ~69 nm in total thickness, at ~300°C (substrate temperature) by sputtering $TiTe_2$ and Sb_2Te_3 targets alternately. The thicknesses of each $TiTe_2$ and Sb_2Te_3 sublayer are ~3 and ~5 nm, respectively. The in situ heating during deposition was necessary for growing high-quality heterostructures because they would otherwise show conventional alloy-like behavior with strong fluctuation and drift in electrical resistance (*35*). The initial direct current-voltage sweep of the pristine (as-fabricated) PCH device exhibited a highly conductive linear ohmic relationship (fig. S1) because all the PCM and CM nanolayers were fully crystallized. For subsequent operations, we observed the threshold-switching behavior (*11*), indicating that the Sb_2Te_3 sublayers were in the amorphous state after each RESET operation (fig. S1). We prepared a GST device with the same geometry for comparison.

Ultralow noise for memory programming

We systematically characterized electrical and structural properties of the PCH devices and PCH thin films. We suppressed the noise of the PCH device: The fluctuations in electrical resistance of both RESET (Fig. 2A) and SET (Fig. 2B) states were strongly reduced compared with those of the GST device. The relative standard deviations of RESET and SET states of the PCH are 1.8 and 0.4%, respectively, which are about one order of magnitude lower than those of the GST device (12.4 and 7.2%, respectively). In conventional PCRAM devices, PCMs are subjected to nonisothermal and nonequilibrium conditions, which result in severe composition variation upon extensive programming owing to long-range diffusional redistribution of constituent elements along the electrical current direction (*11*). Eventually, phase segregation occurs, rendering the device unreliable. In our PCH device, the $TiTe_2$ sublayers with sustained integrity divided the switching component into multiple ~5-nm slabs along the pulsing direction, reducing the possibility and extent of compositional variation and phase segregation. During the quasi–two-dimensional switching in these compartmentalized Sb_2Te_3 nanolayers, the randomness of phase transitions (the stochastic crystallization in particular) was markedly reduced, leading to more consistent resistance contrast and hence better-defined logic states. The simplified switching component by itself, from ternary GST to binary Sb_2Te_3, can contribute to the reduction of stochasticity in crystallization (*9*); however, Sb_2Te_3 alone without $TiTe_2$ multilayers is known to show large noise and poor cycling endurance (*36*).

We used DFT-based molecular dynamics (DFMD) simulations (*34*) to validate from the modeling side the highly confined quasi–two-dimensional phase change. We constructed a periodically repeated $TiTe_2$/Sb_2Te_3 PCH supercell and heated it up to 1300 K. At this high temperature, the Sb_2Te_3 slab quickly melted, but the $TiTe_2$ slab remained intact (fig. S2). The atomic diffusion coefficient profile at 1300 K along the vertical direction, D_v, in the center of the Sb_2Te_3 slab was comparable with that of bulk liquid Sb_2Te_3 but decreased rapidly to zero when approaching the $TiTe_2$ slab (Fig. 2C). We did not observe a single Sb or Te atom penetrating the dense grids formed by $TiTe_2$ during the DFMD simulations at 1300 K for more than ~100 ps. Liquid Sb and Te atoms diffused close to the boundaries, but all bounced back (Fig. 2C). In addition, the spatial gap and the absence of stable bonds formed between

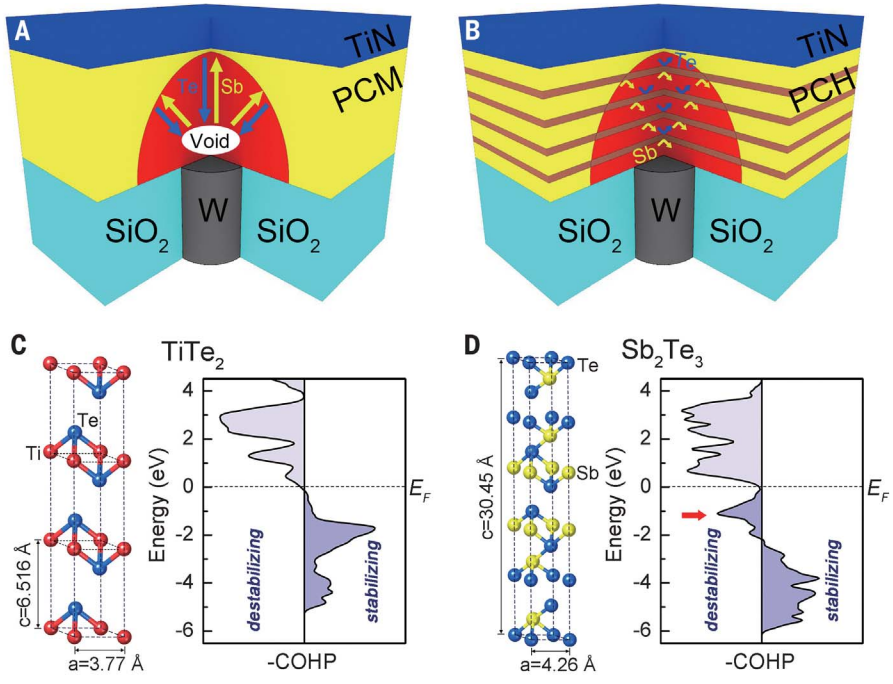

Fig. 1. Material design. (**A** and **B**) Sketch showing the switching of PCM and PCH in mushroom-type PCRAM devices. Yellow areas represent the crystalline state of PCMs, and orange slabs indicate the confinement layers. The red region is the effective programming area in contact with crystalline surroundings, and the arrows denote atomic diffusion occurring in the liquid and supercooled liquid states. The diffusion directions are along that of the input electrical pulse with a given bias polarity. For PCMs, a void could form near BEC upon extensive cycling. (**C** and **D**) The atomic structure and COHP analyses of $TiTe_2$ and Sb_2Te_3 crystals. The left and right parts of the –COHP curve indicate antibonding (destabilizing) and bonding (stabilizing) interactions, respectively. The red arrow marks an antibonding region in Sb_2Te_3 right below its Fermi level E_F.

the Sb_2Te_3 and the $TiTe_2$ slabs confirmed that they are weakly coupled. At the lower temperatures used for programming (500 to 900 K), atomic diffusion across these interslab boundaries is even more unlikely because the kinetic energy of atoms is further reduced.

Using transmission electron microscopy (TEM), we directly observed the preferential amorphization of the PCM layer in the PCH architecture (*34*). Amorphization can be achieved in GST thin films under irradiation of strong electron beams with high accelerating voltage and high beam intensity (*37*). This amorphization route circumvents the evaporation issue that prevents direct observations of melt-quench amorphization in unencapsulated thin films inside TEM. We performed similar in situ irradiation experiments on the PCH thin films on a FEI Titan G2 transmission electron microscope. Many local areas in Sb_2Te_3 slabs turned amorphous after 5 min irradiation, whereas all $TiTe_2$ crystalline slabs remained unchanged (Fig. 2D and fig. S3). The fast Fourier transform (FFT) analyses of typical areas in Sb_2Te_3 slabs (for example, Fig. 2D, boxed regions) showed a clear difference. The vertical stripe-spot pattern for the crystalline phase was in sharp contrast with the halo pattern for the amorphous phase (Fig. 2D). We conducted additional chemical mapping of the PCH thin film (fig. S3) to support the quasi–two-dimensional switching mode.

Ultralow drift in RESET state

The RESET state (obtained with 2.15 V pulses over 20 ns) of the $TiTe_2/Sb_2Te_3$ PCH device (Fig. 3A, inset) showed a very low-resistance drift coefficient (v) of only ~0.002 at room temperature (Fig. 3A, black curve), which is comparable with its SET state (Fig. 3A, red curve). Repeated tests of the RESET states showed consistently low drift of $v < 0.005$. This is in stark contrast with the GST device in its fully amorphous state, where $v \sim 0.11$ (*17*) is more than 50 times higher.

To confirm that the low drift indeed corresponds to the nanoscale amorphous PCM layers, we monitored the cell resistance drift behavior of a T-shaped PCRAM device fabricated based on ~150-nm pure Sb_2Te_3 in contact with a ~190-nm-diameter W BEC (Fig. 3B, inset) at room temperature. The RESET state of this device had a drift coefficient of $v \sim 0.066$ (Fig. 3B), which is about 60% of the GST device of similar size $v \sim 0.11$ (*17*). We scaled down the thickness of the Sb_2Te_3 thin film to ~5 nm and measured its sheet resistance at room temperature. T-shaped PCRAM devices with ~5 nm Sb_2Te_3 were not considered because of the challenge in fabricating and reliably programming (*31*). The sheet resistance of the ~5-nm Sb_2Te_3 thin film, sandwiched by highly resistive SiO_2 layers (Fig. 3C, inset), also showed a very small drift coefficient of $v \sim 0.005$ (Fig. 3C) at room temperature. We further verified using TEM experiments that the ~5-nm Sb_2Te_3 thin film was fully amorphous because we observed no obvious crystallites in the high-resolution TEM image, and the corresponding electron diffraction pattern showed dim halos (Fig. 3D). The electrical response of the ~5-nm amorphous Sb_2Te_3 thin film compares well with the RESET state of ~69-nm PCH device

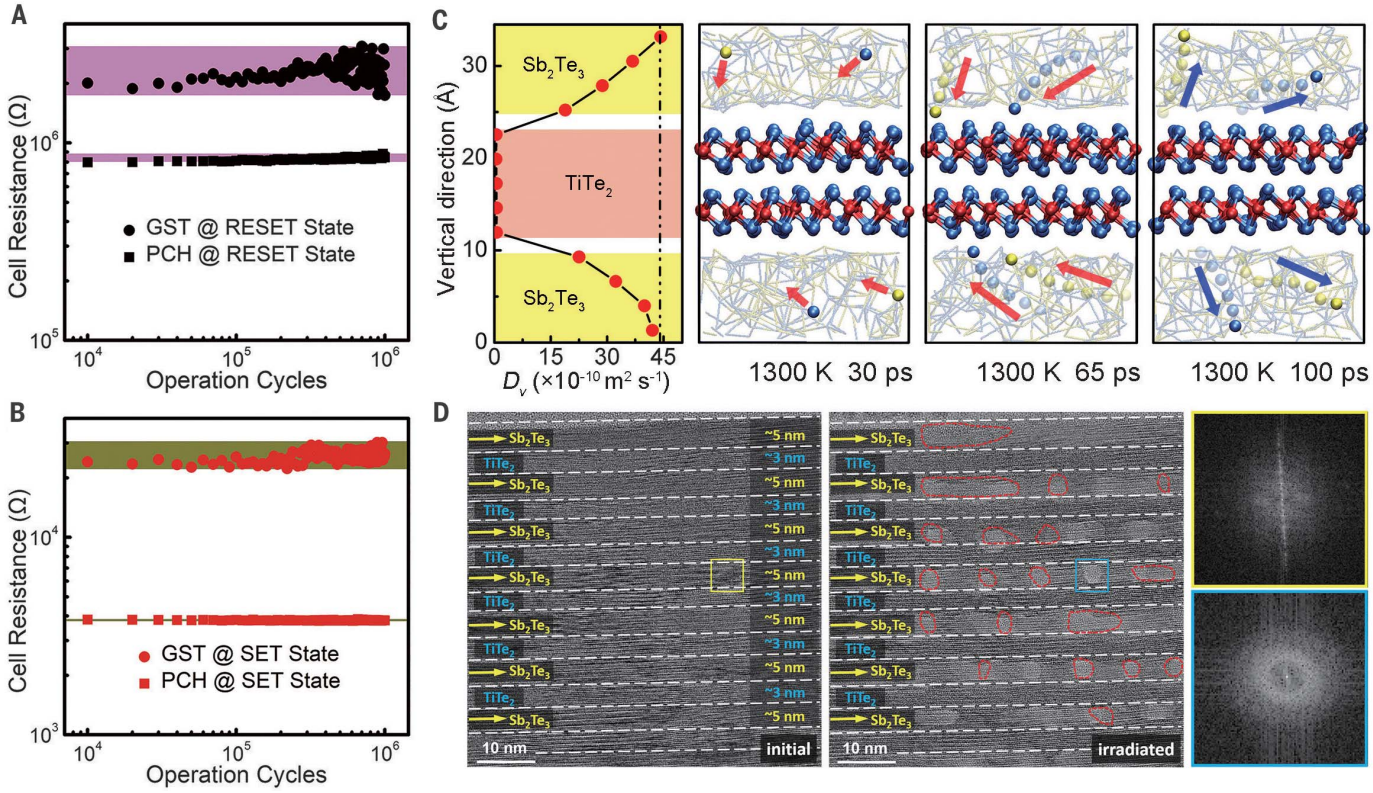

Fig. 2. Prohibited elemental diffusion. (**A** and **B**) Stable resistance values are found for RESET and SET states of the PCH device consistently, in stark contrast with the GST device. The programming was carried out with 10-ns voltage pulses of 2.3 and 1.7 V to RESET and SET, respectively, the PCH device and 50-ns voltage pulses of 5.0 and 2.5 V to RESET and SET, respectively, the GST device. (**C**) The profile of the diffusion coefficient of the heterostructured model along the vertical direction extracted from the DFMD simulations at 1300 K. The dashed line marks the diffusion coefficient of bulk Sb_2Te_3. The diffusion paths of some liquid-like Sb and Te atoms are highlighted. These simulations are subjected to isothermal conditions; therefore, Sb and Te atoms diffuse in random directions, which is different from the situation in devices, in which Sb and Te atoms diffuse oppositely along the pulsing direction. Ti, Sb, and Te atoms are rendered as red, yellow, and blue spheres, respectively. Most of the atoms in the Sb_2Te_3 are indicated by using the chemical bonds formed between them, whereas sticks and balls are used for crystalline $TiTe_2$. (**D**) Under irradiation with strong electron beams for 5 min, parts of the Sb_2Te_3 sublayers of a PCH thin film turn amorphous, whereas the $TiTe_2$ sublayers remain entirely crystalline. A typical area in one Sb_2Te_3 sublayer is analyzed by using FFT, which clearly tells apart the crystalline and amorphous phases.

having multiple ~5-nm Sb_2Te_3 sublayers, but not with the 150-nm-thick Sb_2Te_3 device.

We found two reasons for the low drift in our PCH device. First, the PCH presents simplified chemical bonding and structural motifs in amorphous Sb_2Te_3 compared with closely related PCMs such as GeTe and GST. In the amorphous state of GeTe and GST, the resistance drift is mainly caused by the diminishing content of structural defects such as tetrahedral Ge motifs and the reinforcement of Peierls distortion of (defective-) octahedral motifs (*38*). In amorphous Sb_2Te_3, both Ge and tetrahedral defects are no longer present, hence eliminating one of the driving forces for structural relaxation. This scenario holds for amorphous Sb_2Te_3 in both bulk (*39*) and PCH, as confirmed with our DFMD calculations. Second, the PCH restricts structural relaxation because of nanosize effects. Nanoscale walls were reported to slow down the dynamics of supercooled metallic liquids, restricting the structural relaxation near the walls (*40*). Similarly, the atomic diffusion dynamics of supercooled Sb_2Te_3 liquids decayed rapidly when approaching the $TiTe_2$ walls (Fig. 2C and fig. S4A). The Te–Te antibonding interaction in between the wall and the nearby Te–Sb–Te bonding pairs of Sb_2Te_3 hindered the reinforcement of Peierls distortion toward the walls (fig. S4B). Visible gaps were consistently found between these two sublayers upon quenching the PCH model down to 0 K (fig. S5).

High-accuracy iterative RESET and cumulative SET operations

The key property of PCRAM that enables neuro-inspired computing is its ability to achieve a continuum of electrical resistance values, not just the two basic levels discussed above. The continuous change in electrical resistance can be achieved by either the iterative RESET operation or the cumulative SET operation. Instead of sending a strong voltage pulse for accomplishing a complete RESET operation (Fig. 3A), we applied the RESET pulses with progressively increased amplitude (Fig. 3E, inset). The pulsing scheme resulted in an iterative RESET process with increasing volume of programming region and allowed for multiple intermediate resistance states (Fig. 3E) because the memory cell has a varied crystalline/amorphous ratio (*11*). The GST devices, however, suffered from serious resistance drift (*17*), in which the adjacent resistance states with close magnitude would be difficult to resolve and may even overlap after a certain period of time, leading to decoding errors (*11*). By contrast, we managed to achieve seven intermediate states with consistently low drift coefficients ($v \leq 0.005$) over 1 hour (Fig. 3E) by setting a fixed pulse width of 20 ns and varied pulse amplitude from 1.95 to 2.15 V in our PCH device. We performed the same iterative RESET operation over four additional PCH cells and obtained consistent results with small relative standard deviations below 5.5% (fig. S6). This device property resolves the imprecision and inconsistency issue of PCRAM cells, owing to the suppressed structural relaxation of amorphous Sb_2Te_3 sublayers at room temperature. These 9-level precision memory cells are already well suited for high-accuracy vector-matrix multiplications and pattern classifications (*18*, *27*), and further tuning of the programming parameter and the PCH

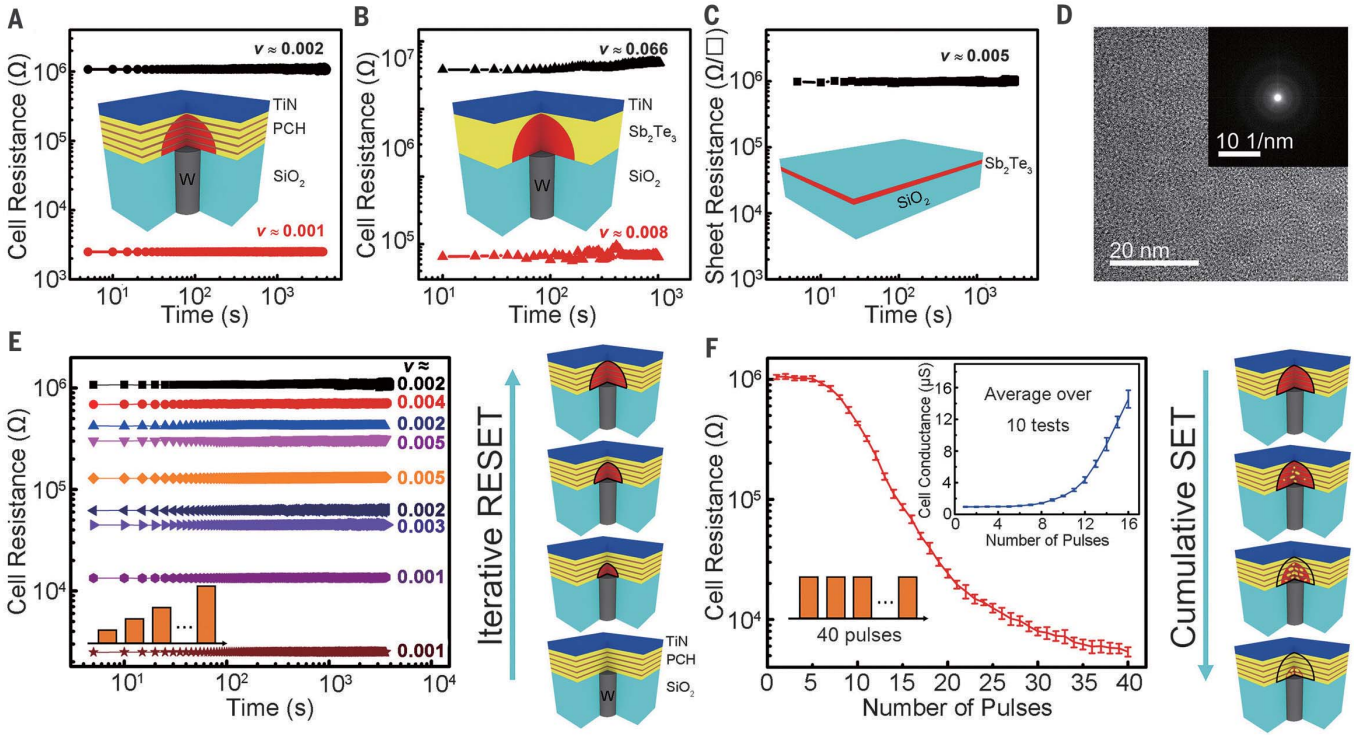

Fig. 3. Suppressed resistance drift. (**A**) Cell resistance as a function of time for the RESET and SET state of the PCH device. (**B**) Cell resistance as a function of time for the RESET and SET state of a ~150-nm-thick Sb_2Te_3 device, with the underlying W plug of ~190 nm in diameter. (**C**) Sheet resistance as a function of time for a ~5-nm-thick amorphous Sb_2Te_3 thin film sandwiched between SiO_2 layers. (Insets) The sketch of the device setup in (A) and (B), and the thin film configuration in (C). All the curves were measured at room temperature. The change of resistance obeys the power law, $R(t) = R_0\,(t/t_0)^v$, where R_0 is the initial resistance at t_0, and v is the fitted resistance drift coefficient. (**D**) The high-resolution TEM image and corresponding electron diffraction pattern of the ~5-nm Sb_2Te_3 film, confirming the film to be in a fully amorphous state. (**E** and **F**) Iterative RESET and cumulative SET operations. (Insets) The pulse waveforms. The sketch plots show the size of programming areas (black lines) and the change in effective amorphous volumes (red areas). The iterative RESET operation was done by setting a fixed pulse width of 20 ns and varied pulse amplitude from 1.95 to 2.15 V. The cumulative SET operation was done by sending a train of 40 voltage pulses with the same magnitude (0.8 V) and the same width (100 ns). The same operation was repeated 10 times. The top inset in (F) shows the computed conductance (with standard deviation) converted from the resistance data.

geometry should be able to readily increase the number of reliable intermediate states (fig. S7).

Higher-level in-memory (such as machine-learning) tasks and integration of neural networks with and without emulations of synapses and neurons are in general demanding, in terms of maximum tolerable fluctuations, on cumulative SET operation (*29*). A cumulative SET operation is done by sending a train of narrow voltage pulses with the same low amplitude (Fig. 3F, inset), corresponding to programming areas of the same size (Fig. 3F, inside the black lines). Unlike iterative RESET, in which the melt-quench amorphization is abrupt and the resistance of multilevel states changes as a function of the amorphous/crystalline ratio, the cumulative SET operation is accomplished through incubation of crystal nuclei, their subsequent growth, and parallel mushroom boundary shrinkage, leading to a nonlinear reduction in cell resistance (Fig. 3F).

We performed the cumulative SET operation using a train of 40 identical voltage pulses (0.8 V and 100 ns of each pulse) on the same PCH cell 10 times. As designed, the multiple $TiTe_2$ walls prevent the formation of polycrystalline grains vertically because the typical grain size of nucleation-type PCMs is 5 to 20 nm. In addition, similar local atomic motifs in these walls may promote crystallization of Sb_2Te_3 sublayers through potential interface nucleation. As expected, consistent resistance (with ≲10% fluctuation) is found at each and every point along the path from the RESET state to the SET state (covering the full resistance contrast window of more than 2 orders of magnitude), for the 10 tests of the same PCH device (Fig. 3F and fig. S8). We also computed the conductance, because neural network emulations use this variable, and set a similar window below 15 μS (Fig. 3F, top inset) to compare with the GST devices of similar configuration (*29*). The relative standard deviation in conductance is below 9% for a single PCH device, in contrast with the GST device (>40%) (*29*). We carried out the same cumulative SET operation over four additional PCH cells, and the intercell fluctuation in conductance was below 11% (fig. S9). We attribute the highly repeatable conductance of the PCH device to the reduced structural variability of crystallization (including the size, volume fraction, and crystallographic orientation of the crystallized grains) and the decreased pulse-to-pulse composition variation, made possible by the robust confinement layers. Advances in this direction are highly promising for many machine-learning tasks, such as unsupervised learning of temporal correlations between binary stochastic processes (*28*). Further reduction in the randomness associated with crystallization may be possible by tuning the thickness and stoichiometry (*9*) of the PCM nanolayers.

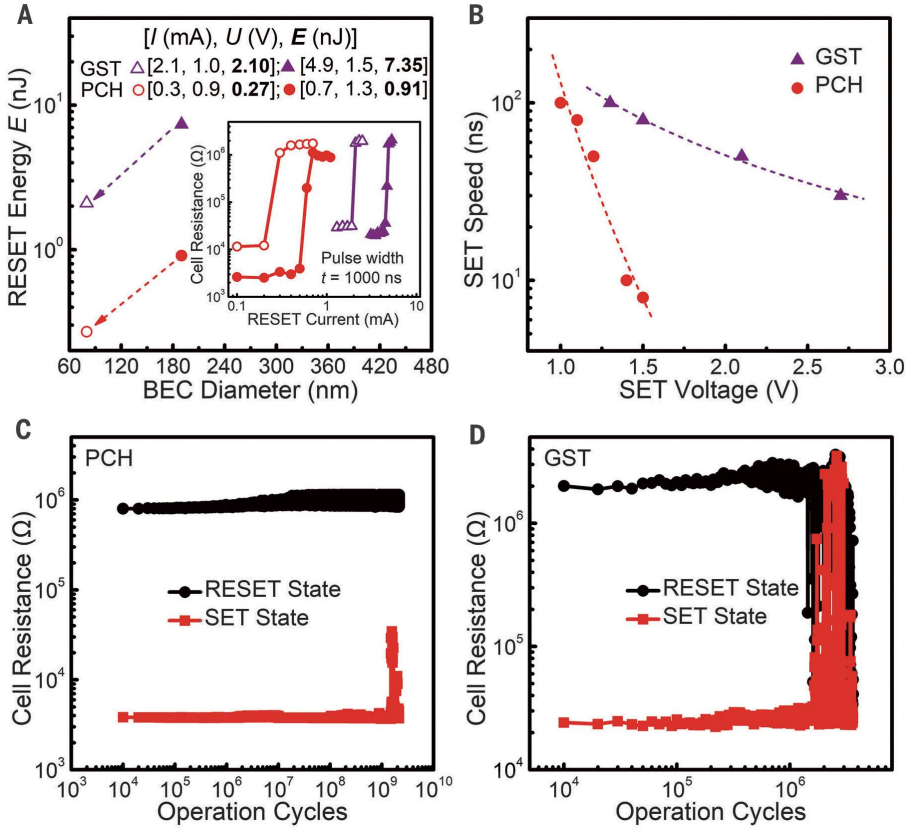

Fig. 4. Improved RESET energy, SET speed, and cycling endurance. (**A**) RESET energy (*E*) as a function of BEC diameter for the GST and PCH devices. (Inset) Cell resistance versus RESET current (*I*) curves with a fixed pulse width of 1000 ns (*t*) for both devices with different BEC (Φ = 80, 190 nm). Transient RESET voltage (*U*) across the device is recorded once the RESET state is reached. The input RESET energy (*E*) is calculated as $E = I \times U \times t$. *E* depends on *t*, which can be reduced to subnanosecond level, resulting in picojoule-level RESET energies. (**B**) SET speed as a function of voltage bias for PCH and GST devices with the same geometry (190 nm in BEC diameter). The PCH device can accomplish SET operations within 8 ns at 1.5 V. (**C**) Approximately 2×10^9 cycling endurance of the PCH device: SET (at 1.7 V) and RESET (at 2.3 V) with 10-ns voltage pulses. (**D**) Approximately 1×10^6 cycling endurance of the GST device: SET (at 2.5 V) and RESET (at 5.0 V) with 50-ns voltage pulses.

Improved programming energy, speed, and cycling endurance

Our PCH architecture leads to much improved RESET energy, SET speed, and cycling endurance compared with those of conventional GST devices. The required voltage bias for RESET operations (Fig. 4A) in the PCH device is ~2.0 to 2.5 V when using sub-10-ns voltage pulses, and much lower than that for the GST device, ~3.5 to 6.1 V when using several tens of nanosecond voltage pulses, meeting the low-bias criterion for mass-produced chips (*41*). To make an accurate estimate of RESET energies, we used a very wide constant electric current pulse of 1000 ns (*t*). The RESET energy (*E*) is then calculated as $E = I \times U \times t$, resulting in 0.91 and 7.35 nJ for the PCH and GST device, respectively (where *I* is the RESET current and *U* is the RESET voltage) (Fig. 4A). Decreasing the diameter Φ of the BEC from 190 to 80 nm, the RESET energy reduces to 0.27 and 2.10 nJ, respectively. We partly attribute this dramatic reduction in power consumption by more than 87% to the partial melting in the PCH device, where ~40% of the PCH film is crystalline $TiTe_2$ and stays unchanged. The confinement $TiTe_2$ layers are also thermally resistive, suppressing the through-plane heat loss during programming. The RESET operation of the PCH device can be completed on the nanosecond level under low bias, which reduces the RESET energies to the picojoule level. Improved power consumption was also reported in a $GeTe/Sb_2Te_3$ superlattice (*42*), although its switching mechanism is still under active debate (*43*, *44*).

We improved both the SET time and SET voltage of the PCH device over the GST device (Fig. 4B and fig. S10). In particular, the PCH device reached ~8 ns SET time at ~1.5 V, which fulfills the sub-10-ns speed and the low-bias requirements for DRAM-like applications. In comparison, at ~1.5 V the GST device needed ~80 ns for SET operations. Similar to RESET operations, the enhanced thermal efficiency by

the confinement layers and the partial switching manner of the memory cell work together to reduce the SET time, bias, and energy. Moreover, the $TiTe_2$ layers have a similar atomic arrangement as that of crystalline Sb_2Te_3 and may serve as potential heterogeneous nucleation sites to facilitate the crystallization of Sb_2Te_3 at elevated temperatures. The enhanced crystallization tendency is evidenced by the fact that a similar device with Sb_2Te_3 film (~150 nm) took ~60 ns to complete the SET operations at ~1.5 V and needed ~4 V to reach ~8 ns (*9*). This difference indicates a reduced energy barrier for crystallization in the presence of the $TiTe_2$ layers. Our DFT energy analyses also suggest favorable interfacial interaction for crystallization between the crystalline $TiTe_2$ slab and the amorphous Sb_2Te_3 slab (fig. S5).

Regarding the cycling endurance, extensive cycles of high-bias voltage pulses would trigger long-distance atomic migrations of Sb (Ge) and Te elements in opposite (vertical) directions, giving rise to elemental segregation as well as void formation near the bottom electrode (*11*). The best-performing PCH device showed a cycling endurance of ~2×10^9 (Fig. 4C), which is three orders of magnitude longer than the ~1×10^6 cycles of the GST device with the same geometry (Fig. 4D). Additional examples consistently showing low noise and endurance up to 10^8 to 10^9 cycles are displayed in fig. S11. We attribute the extended cycling life to the smaller bias and energy requested for rapid programming of the PCH device and the effective role of the rigid and dense $TiTe_2$ walls in reducing the possibility of the long-range elemental diffusion along the pulsing direction. The intrinsic materials innovation offered by our PCH architecture should be easily integrated with other extrinsic device and programming strategies. Examples of the latter include the shrinking down of the switching volume by using a fabrication line of industrial quality that can increase the cycling endurance of GST devices to ~10^{12} cycles (*45*) and programming schemes that trigger self-healing (backward elemental migration) of degraded GST devices upon reversing the polarity of programming pulses (*46*).

Conclusion

We have demonstrated an innovative design of PCH architecture that offers multiple performance benefits over traditional PCRAM devices—in particular, the substantially reduced noise and drift in resistance states. The advantages originated from the suppressed compositional and structural variability in phase transition cycles and enabled well-controlled iterative RESET and cumulative SET operations. The PCH approach is amenable to industrial production because the multilayer deposition does not substantially increase the fabrication cost or demand complex procedure, making it relatively easy to be incorporated into state-of-the-art device setups for applications such as high-performance neuro-inspired computing. In addition, our discovery opens the door for nonvolatile DRAM-like memories (*9*) with stable multilevel storage capacity. Besides potential applications in memory and computing, many two-dimensional transition-metal dichalcogenides are topologically nontrivial (*47*), with antimony telluride being a prototypical topological insulator (*48*). Alternate stacking of these nanolayers to form heterostructures (*49*) may lead to new physics phenomena that are also worth exploring.

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SUPPLEMENTARY MATERIALS

science.sciencemag.org/content/366/6462/210/suppl/DC1
Materials and Methods
Figs. S1 to S11
References (*50*–*60*)

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Phase-change heterostructure enables ultralow noise and drift for memory operation

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Getting more bits out of PCRAM

Phase-change random access memory (PCRAM) has the ability to both store and process information. It also suffers from noise and electrical drift due to damage that accumulates during the cycling process. Ding *et al.* developed a phase-change heterostructure where a phase-change material is separated by a confinement material, creating an alternating stack (see the Perspective by Gholipour). This architecture results in ultralow noise, lower drift, and stable multilevel storage capacity, which are potentially useful for new forms of computing.

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